What is claimed is:

1. A current-voltage transforming circuit comprising:

a photo detector generating a photo current in response to a photo signal inputted into the photo detector;

an amplifier amplifying the photo current received from the photo detector;

an emitter follower coupled to the amplifier;

an output buffer coupled to the emitter;

a current detecting limiter unit having an input terminal and an output terminal to output a limiter current when an output current of the amplifier is greater than a predetermined reference value; and

a feedback resistor coupled between the photo detector and the amplifier.

2. The circuit of claim 1, wherein the input terminal of the current detecting limiter unit is coupled to a junction between the emitter follower and the output buffer.

3. The circuit of claim 1, wherein the input terminal of the current detecting limiter unit is coupled to an output terminal of the output buffer.

4. The circuit of claim 1, wherein the output terminal of the current detecting limiter unit is coupled to an input of the amplifier.

5. The circuit of claim 1, wherein the output terminal of the current detecting limiter unit is coupled to ground.

6. The circuit of claim 1, wherein the amplifier comprises:

a differential amplifier receiving an input voltage of the photo current generated from the photo detector and a reference voltage.

7. The circuit of claim 6, wherein the differential amplifier comprises a pair of differential transistors and first and second biases supplied to the differential transistors.

8. The circuit of claim 1, wherein the current detecting limiter unit comprises:

a voltage source;

first and second resistors;

a first transistor having collector coupled to the voltage source, a base receiving the output current, and an emitter coupled to the first and second resistors; and.

a second transistor having a collector coupled to receive a current from one of the emitter follower and the output buffer, an emitter coupled to output the limiter current, and a base coupled to a junction between the first and second resistors.

9. The circuit of claim 8, wherein the first and second transistors comprise:

an NPN type transistor.

10. The circuit of claim 8, wherein the second transistor is turned on when $V_{b2} > V_{REF} + V_{beq2}$ where V_{b2} is a voltage of the junction, V_{REF} is a reference voltage, and V_{beq2} is a base and emitter voltage of the second transistor.

11. The circuit of claim 1, wherein the output terminal of the current detecting limiter unit comprises:

first and second sub-output terminals coupled to the amplifier and ground, respectively.

12. The circuit of claim 11, wherein the current detecting limiter unit comprises:

a voltage source;

first and second resistors;

a first transistor having collector coupled to the voltage source, a base receiving the output current, and an emitter coupled to the first and second resistors; and.

a second transistor having a collector coupled to receive a current from one of the emitter follower and the output buffer, an emitter coupled to the first sub-output terminal, and a base coupled to a junction between the first and second resistors.

13. The circuit of claim 11, wherein the current detecting limiter unit comprises:

a voltage source;

first and second resistors;

a first transistor having collector coupled to the voltage source, a base receiving the output current, and an emitter coupled to the first and second resistors;

a second transistor having a collector coupled to receive a current from one of the emitter follower and the output buffer, an emitter coupled to the first sub-output terminal, and a base coupled to a junction between the first and second resistors; and

a third transistor having a collector coupled to receive the current from one of the emitter follower and the output buffer, an emitter coupled to the second sub-output terminal, and a base coupled to a junction between the first and second resistors.

14. The circuit of claim 11, wherein the second

resistor comprises:

a variable resistor.

15. The circuit of claim 1, the current detecting limiter unit comprises:

a voltage source;

first and second resistors;

a first transistor having collector coupled to the voltage source and the first resistor, a base coupled to ground and the second resistor, and an emitter coupled to receive the photo current; and.

a second transistor having an emitter to receive a current from one of the emitter follower and the output buffer, a collector coupled to output the limiter current, and a base coupled to a junction between the first resistor and the first transistor.

16. The circuit of claim 15, wherein the first transistor comprises an NPN type transistor, and the second transistor comprises a PNP type transistor.

17. The circuit of claim15, wherein the current detecting limiter unit comprises:

a third transistor having a base connected to the collector of the second transistor, a collector connected to the emitter of the second transistor, and an emitter coupled to output the limiter current.

18. The circuit of claim 17, wherein the third transistor comprises an NPN type transistor.

19. A current-voltage transforming circuit used with a photo detector integrated circuit of a disc recording and/or reading apparatus, comprising:

a photo detector generating a photo current in response to a photo signal inputted into the photo detector;

a trans-impedance amplifier converting and amplifying the photo current to generate an output voltage, and generating first and second currents; and

a current detecting limiter generating a limiter current in response to the first and second currents so that the trans-impedance amplifier is prevented.

20. The circuit of claim 19, wherein the trans-impedance amplifier comprises:

an amplifier amplifying the photo current received from the photo detector;

an emitter follower coupled to the amplifier;

an output buffer coupled to the emitter to generate the output voltage; and

a feedback resistor coupled between the output buffer and the amplifier so that the photo current is converted into the output voltage.

22. The circuit of claim 21, wherein the first and second currents are generated from one of a first junction between the amplifier and the emitter follower, a second junction between the emitter follower and the output buffer, and an output terminal of the output buffer.

23. The circuit of claim 21, wherein the limiter current is outputted to one of a junction between the output buffer and the amplifier and a reference potential.

24. The circuit of claim 21, wherein the first and second currents are different from each other.

25. The circuit of claim 21, wherein the current detecting limiter unit outputs one of the first and second

currents as the limiter current when the other one of the first and second currents is greater than a predetermined reference value.

26. A disc recording and/or reading apparatus having a current-voltage transforming circuit of a photo detector integrated circuit, comprising:

a photo detector generating a photo current in response to a photo signal inputted into the photo detector;

a trans-impedance amplifier converting and amplifying the photo current to generate an output voltage, and generating first and second currents; and

a current detecting limiter generating a limiter current in response to the first and second currents so that the trans-impedance amplifier is prevented.

27. The apparatus of claim 26, wherein the trans-impedance amplifier comprises:

an amplifier amplifying the photo current received from the photo detector;

an emitter follower coupled to the amplifier;

an output buffer coupled to the emitter to generate the output voltage; and

a feedback resistor coupled between the output buffer and the amplifier so that the photo current is converted into the output voltage.

28. The apparatus of claim 26, wherein the first and second currents are generated from one of a first junction between the amplifier and the emitter follower, a second junction between the emitter follower and the output buffer, and an output terminal of the output buffer.

29. The apparatus of claim 26, wherein the limiter

current is outputted to one of a junction between the output buffer and the amplifier and a reference potential.

30. The apparatus of claim 26, wherein the first and second currents are different from each other.

31. The apparatus of claim 26, wherein the current detecting limiter unit outputs one of the first and second currents as the limiter current when the other one of the first and second currents is greater than a predetermined reference value.